REMARKS

The following remarks are made in response to the Non-Final Office Action mailed April 6, 2007. Claims 8-21 have been allowed. Claims 1, 5, and 22-28 were rejected. Claims 2-4, 6 and 7 have been objected to. Claims 1-28 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 1, 5, 22-23, and 25-28 under 35 U.S.C. § 102(e) as being anticipated by the Aung et al. et al. U.S. Patent Application Publication No. 2003/0212939.

Independent claims 1, 22, 25, 26, 27, and 28 relate to clock data recovery (CDR)-based clock synthesis. A clock signal is synthesized by performing a CDR operation on a clock source signal, in particular, on a potentially noisy clock source signal having a fixed transition density. The CDR operation produces a desired clock signal in response to this clock source signal. Each of independent claims 1, 22, and 25-28 defines features relating to clock synthesis by performing a CDR operation.

The Examiner rejected independent claims 1, 22, and 25-28 based on the Aung et al. publication and in particular Figure 1 and the corresponding text and Figure 7 and the corresponding text. Applicant, however, respectfully submits that the Figure 1 embodiment and the Figure 7 embodiment disclosed in the Aung et al. publication are two completely distinct embodiments. Moreover, there is no teaching or suggestion in the Aung et al. publication to combine these individual embodiments. In addition, even if the embodiment of Figure 1 and the embodiment of Figure 7 were combined, this combination would not result in the invention of independent claims 1, 22, and 25-28.

Independent claim 1 claims a clock synthesizer apparatus comprising a CDR circuit including a serial data input. The CDR circuit is operable when a serial data stream is applied via the serial data input for recovering a clock signal from the serial data stream. A clock source input receives a clock source signal having a fixed transition density. The clock source input is coupled to the serial data input for applying the clock source signal to the CDR circuit. The CDR circuit is responsive to the clock source signal received at the serial data input to produce a

desired clock signal. All of these recited limitations of independent claim 1 are not taught or suggested by the Aung et al. publication.

One embodiment of such a clock synthesizer apparatus, as defined in independent claim 1, is illustrated in Figure 2 of the present application. In the embodiment illustrated in Figure 2, a CDR circuit CDR2 receives a clock source signal having a fixed transition density (e.g., TXCKSRC). The CDR circuit CDR2 produces via a CDR operation, a desired clock signal (e.g., in Figure 2 a transmit clock for a serializer).

In contrast to independent claim 1, the Aung et al. publication discloses CDR circuitry associated with programmable logic device (PLD) circuitry. The disclosure of the Aung et al. publication focuses on PLDs and the problems associated with PLDs. The Aung et al. publication discloses using CDR signaling in combination with such PLDs. CDR signaling, in this context, means that the clock signal information is embedded in a data signal, and at a receiver side, the clock signal is recovered from the data signal for use in properly processing the data of the data signal. For example, see paragraph [0003] of the Aung et al. publication.

In particular, Figure 1 of the Aung et al. publication illustrates CDR receiver circuitry. In Figure 1 of the Aung et al. publication, receiver 40 includes CDR circuitry 50. CDR circuitry 50 is only conventional CDR circuitry which uses a received reference clock in a serial data signal to extract from the serial data signal a clock signal and a data signal. However, this CDR circuitry 50 does not have a clock source input coupled to the serial data input of the CDR circuitry 50, and in particular, the CDR circuitry 50 is not responsive to a clock source signal received at the serial data input thereof for producing a desired clock signal, as recited in independent claim 1. Rather, in Figure 1 of the Aung et al. publication, the CDR circuitry 50 is responsive to the reference clock signal, which is received at a separate clock input of the CDR circuitry 50.

By contrast, Figure 7 of the Aung et al. publication illustrates a transmitter of a CDR signal. In Figure 7 of the Aung et al. publication, transmitter 320 of the CDR signal does not have any CDR circuitry, and only uses a PLL 100 which does not have any serial data input, as recited in independent claim 1.

In view of the above, independent claim 1 is not taught or suggested by the Aung et al. publication.

Independent claim 22 claims a method of synthesizing a clock signal comprising providing a clock source signal having fixed data transition density and performing a CDR operation on the clock source signal to produce a desired clock signal in response to the clock source signal.

As described above, the Aung et al. publication only discloses performing a conventional CDR operation on a serial data stream so as to recover from the serial data stream a clock signal and a data signal by using a reference clock signal (see e.g., Figure 1 and corresponding text of the Aung et al. publication). The Aung et al. publication does not teach or suggest performing a CDR operation on a clock source signal having a fixed transition density to produce a desired clock signal, as recited in independent claim 22. Rather, the Aung et al. publication only discloses performing a CDR operation to recover a clock signal from the CDR data stream.

In view of the above, independent claim 22 is not taught or suggested by the Aung et al. publication.

Independent claim 25 claims a serial data transceiver apparatus comprising means for deserializing an input serial data stream, means for converting parallel data into an output serial data stream based on a transmit serialization clock signal, and means for producing the transmit serialization clock signal by applying a CDR operation to a clock source signal.

The above recited limitations of independent claim 25 are not taught or suggested by the Aung et al. publication. In particular, as recited in independent claim 25, the desired clock signal is employed as a transmit serialization clock signal for converting parallel data into an output serial data stream and for transmitting the serial data stream. The Aung et al. publication does not teach or suggest producing a desired clock signal, in particular a desired transmit serialization clock signal, by applying a CDR operation to a clock source signal, as recited in independent claim 25.

Furthermore, the Aung et al. publication does not even disclose a transceiver apparatus. Instead, the Aung et al. publication discloses PLDs in combination with CDR signaling. For example, Figure 1 and the corresponding text of the Aung et al. publication only discloses CDR

receiver circuitry and Figure 7 and the corresponding text of the Aung et al. publication only discloses a transmitter of a CDR signal.

In view of the above, independent claim 25 is not taught or suggested by the Aung et al. publication.

Independent claim 26 claims a serial data transceiver apparatus comprising a received data input for receiving an input serial data stream. A CDR circuit is coupled to the received data input for recovering a receive clock signal from the input serial data stream. A data serializer converts parallel data into an output serial data stream. The data serializer has a clock input for receiving a transmit serialization clock signal. The data serializer produces the output serial data stream based on the transmit serialization clock signal. A clock synthesizer apparatus is coupled to the clock input for providing the transmit serialization clock signal. The CDR circuit and the clock synthesizer apparatus have respective PLL clock inputs. Each of the PLL clock inputs receives first and second PLL clocks. The PLL has an output for providing the first and second PLL clocks. The CDR circuit and the clock synthesizer apparatus each have the PLL clock input coupled to the PLL output for receiving the first and second PLL clocks.

All of the above recited limitations of independent claim 26 are not taught or suggested by the Aung et al. publication. In particular, the serial data transceiver apparatus recited in independent claim 26 employs a single PLL, where the first and second PLL clock signal generated by the PLL are supplied both to the CDR circuit for recovering the received clock signal from the input serial data stream and to the clock synthesizer apparatus for generating the transmit serialization clock signal for the data serializer.

As discussed above, the Aung et al. publication does not even disclose a serial data transceiver apparatus. Figure 1 and the corresponding text of the Aung et al. publication only discloses CDR receiver circuitry in combination with a PLD, and Figure 7 and corresponding text of the Aung et al. publication only discloses a transmitter of a CDR signal in combination with a PLD. The Aung et al. publication does not disclose the combination of a receive data path and a transmit data path in the structure defined by the above limitations of independent claim 26.

Furthermore, the Aung et al. publication does not teach or suggest that only one single PLL could be used to generate both the PLL clock signals for the received data path and the PLL clock signals for the transmit data path, as recited in independent claim 26. More specifically, the Aung et al. publication does not teach or suggest generating with a single PLL, the PLL clock signals for both the CDR circuit of the receive data path and the clock synthesizer apparatus of the transmit data path, as recited in independent claim 26.

In view of the above, independent claim 26 is not taught or suggested by the Aung et al. publication.

Independent claim 27 claims a serial data transceiver apparatus comprising means for recovering a received clock signal from the input serial data stream based on first and second PLL clocks, means for producing a transmit serialization clock signal based on the first and second PLL clocks, and means for converting parallel data into an output serial data stream based on the transmit serialization clock signal.

These recited limitations of independent claim 27 are not taught or suggested by the Aung et al publication. In particular, the Aung et al. publication does not disclose employing the same first and second PLL clocks for recovering a received clock signal from an input serial data stream and for producing a transmit serialization clock signal as recited in independent claim 27. Therefore, independent claim 27 is not taught or suggested by the Aung et al. publication.

Independent claim 28 claims the method of transmitting and receiving serial data comprising recovering a received clock signal from an input serial data stream based on first and second PLL clocks, producing a transmit serialization clock signal based on the first and second PLL clocks, and converting parallel data into an output serial data stream based on the transmit serialization clock signal.

The Aung et al. publication does not teach or suggest all of these recited limitations of independent claim 28. In particular, independent claim 28 defines that the receive clock signals and the transmit serialization clock signal are generated based on the same first and second PLL clock signals, which is not taught or suggested by the Aung et al. publication.

Furthermore, dependent claim 5 further defines patentably distinct independent claim 1. Dependent claim 23 further defines patentably distinct independent claim 22. Therefore, these dependent claims are also believed to be allowable.

Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 102(e) rejection to claims 1, 5, 22-23 and 25-28, and request allowance of these claims.

Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claim 24 under 35 U.S.C. § 103(a) as being unpatentable over the Aung et al. U.S. Publication No. 2003/0212930.

Dependent claim 24 further defines patentably distinct independent claim 22. Therefore, this dependent claim is also believed to be allowable.

Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection to claim 24, and request allowance of this claim.

Allowable Subject Matter

Claims 8-21 have been allowed.

The Examiner objected to claims 2-4 and 6-7 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

Applicant agrees with the Examiner that claims 2-4 and 6-7 would be allowable if rewritten in independent form. However, as dependent claims 2-4 and 6-7 further define patentaby distinct independent claim 1, these dependent claims are believe to be allowable in dependent form. Therefore, Applicant respectfully requests the objections to claims 2-4 and 6-7 be removed and that these claims be allowed in dependent form.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-28 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-28 are respectfully requested.

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Patrick Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

Dicke, Billig & Czaja
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402

Respectfully submitted,

Hamid Partovi et al.,

By their attorneys,

DICKE, BILLIG & CZAJA, PLLC
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402
Telephone: (612) 573-2003
Facsimile: (612) 573-2005

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PGB:cmj:dmw:cms

/Patrick G. Billig/
Patrick G. Billig
Reg. No. 38,080